What Is Claimed Is:

1. A method, comprising:

generating a checkpoint at one of a plurality of branches in a checkpoint buffer having at least one checkpoint buffer entry, wherein said plurality of branches include one or more instructions;

generating a counter for said at least one checkpoint buffer entry;

associating said one or more instructions with said checkpoint; and

tracking with said counter said one or more instructions associated with said checkpoint.

2. The method of claim 1, further comprising:

accessing said checkpoint at the occurrence of a recovery event;

restoring an architectural state associated with said checkpoint; and

processing at least one instruction from said one or more instructions associated with said checkpoint.

3. The method of claim 1, further comprising:

reclaiming said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

4. The method of claim 1, said generating a checkpoint further comprising:

estimating a misprediction probability for one or more of said plurality of branches.

5. The method of claim 1, wherein generating said checkpoint occurs when a checkpoint buffer entry is available.

6. The method of claim 1, further comprising processing beyond said plurality of branches without generating said checkpoint when said checkpoint buffer entry is not available.

7. The method of claim 1, wherein said tracking step further comprises:

incrementing said counter when said one or more instructions is allocated; and

decrementing said counter when said one or more instructions completes execution.

8. The method of claim 1, wherein checkpoints are reclaimed in a first-in-first-out order.

9. The method of claim 1, wherein an oldest checkpoint is reclaimed when a subsequent checkpoint is generated.

10. The method of claim 1, wherein one or more of said checkpoints are combined based upon the misprediction probability of said one or more instructions associated with said one or more of said checkpoints.

11. An apparatus, comprising:

a branch predictor to generate a checkpoint at one of a plurality of branches; and

a checkpoint buffer to store one or more counters, wherein said checkpoint buffer has at least one checkpoint buffer entry;

wherein said branch predictor generates a counter for said at least one checkpoint buffer entry to associate one or more instructions with said checkpoint, and wherein said branch predictor tracks said one or more instructions using said counter.

12. The apparatus of claim 11, wherein said branch predictor accesses said checkpoint at the occurrence of a recovery event, restores an architectural state associated with said checkpoint, and processes at least one instruction from said one or more instructions associated with said checkpoint.

13. The apparatus of claim 11, wherein said branch predictor reclaims said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

14. The apparatus of claim 11, further comprising:

a branch confidence estimator to estimate a misprediction probability for one or more of said plurality of branches.

15. The apparatus of claim 14, wherein said branch confidence estimator accesses misprediction history information.

16. The apparatus of claim 15, wherein said branch confidence estimator further comprises a counter associated with said branch having a high misprediction probability and adapted to track when said branch is mispredicted.

17. The apparatus of claim 11, further comprising:

a recovery buffer to store previously executed instructions for use in misprediction recovery.

18. The apparatus of claim 11, wherein said branch predictor further comprises a branch target buffer to store said one or more instructions.

19. A system, comprising:

a processor including a branch predictor to generate a checkpoint at one of a plurality of branches, and a checkpoint buffer to store one or more counters, wherein said checkpoint buffer has at least one checkpoint buffer entry, wherein said branch predictor generates a counter for said at least one checkpoint buffer entry to associate one or more instructions with said checkpoint, and wherein said branch predictor tracks said one or more instructions using said counter;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

20. The system of claim 19, wherein said branch predictor accesses said checkpoint at the occurrence of a recovery event, restores an architectural state associated with said checkpoint, and processes at least one instruction from said one or more instructions associated with said checkpoint.

21. The system of claim 19, wherein said branch predictor reclaims said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

22. The system of claim 19, further comprising:

a branch confidence estimator to estimate a misprediction probability for one or more of said plurality of branches.

23. The system of claim 22, wherein said branch confidence estimator accesses misprediction history information.

24. The system of claim 23, wherein said branch confidence estimator further comprises a counter associated with said branch having a high misprediction probability and adapted to track when said branch is mispredicted.

25. The system of claim 19, further comprising:

a recovery buffer to store previously executed instructions for use in misprediction recovery.

26. The system of claim 19, wherein said branch predictor further comprises a branch target buffer to store said one or more instructions.